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1 [Distributed scheduling algorithms to improve the performance of parallel data transfers](#)



Dannie Durand, Ravi Jain, David Tseytlin

 September 1994 **ACM SIGARCH Computer Architecture News**, Volume 22 Issue 4

Publisher: ACM Press

 Full text available: [pdf\(588.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

The cost of data transfers, and in particular of I/O operations, is a growing problem in parallel computing. A promising approach to alleviating this bottleneck is to schedule parallel I/O operations explicitly. We develop a class of decentralized algorithms for scheduling parallel I/O operations, where the objective is to reduce the time required to complete a given set of transfers. These algorithms, based on edge-coloring and matching of bipartite graphs, rely upon simple heuristics to obtain ...

2 [A scheduling and allocation method to reduce data transfer time by dynamic reconfiguration](#)



Kazuhito Ito

 January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation ASP-DAC '00**

Publisher: ACM Press

 Full text available: [pdf\(92.93 KB\)](#) Additional Information: [full citation](#), [references](#)

3 [The DT-model: high-level synthesis using data transfers](#)



Shantanu Tarafdar, Miriam Leeser

 May 1998 **Proceedings of the 35th annual conference on Design automation DAC '98**


Publisher: ACM Press

 Full text available: [pdf\(179.39 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present a new model for formulating the classic HLS sub-problems: scheduling, allocation, and binding. The model is unique in its use of data-transfers as the basic entity in synthesis. A data transfer represents the movement of one instance of data and contains the operation sourcing the data and all the operations using it. Our model compels the storage architecture of the design to be optimized concurrently with the execution unit. We have built a high-level synthesis system, Mi ...

Keywords: high-level synthesis, telecommunication



4 Integrating floorplanning in data-transfer based high-level synthesis

 Shantanu Tarafdar, Miriam Leeser, Zixin Yin
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design ICCAD '98**
Publisher: ACM Press
Full text available:  pdf(739.34 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

5 Scheduling data transfers in a network and the set scheduling problem

 Ashish Goel, Monika R. Henzinger, Serge Plotkin, Eva Tardos
May 1999 **Proceedings of the thirty-first annual ACM symposium on Theory of computing STOC '99**
Publisher: ACM Press
Full text available:  pdf(808.96 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)


6 Introspection: A register transfer level technique for cocurrent error detection and diagnosis in data dominated designs

 Ramesh Karri, Balakrishnan Iyer
October 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 4
Publisher: ACM Press
Full text available:  pdf(211.42 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We report a register transfer level technique for concurrent error detection and diagnosis in data dominated designs called *Introspection*. Introspection uses idle computation cycles in the data path and idle data transfer cycles in the interconnection network in a synergistic fashion for concurrent error detection and diagnosis (CEDD). The resulting on-chip fault latencies are one ten-thousandth (10^{-4}) of previously reported system level concurrent error detection and diagnosis ...

Keywords: Concurrent error detection, on line testing, register transfer level



7 Efficient rate-controlled bulk data transfer using multiple multicast groups

Supratik Bhattacharyya, James F. Kurose, Don Towsley, Ramesh Nagarajan
December 2003 **IEEE/ACM Transactions on Networking (TON)**, Volume 11 Issue 6
Publisher: IEEE Press
Full text available:  pdf(637.84 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Controlling the rate of bulk data multicast to a large number of receivers is difficult, due to the heterogeneity among the end systems' capabilities and their available network bandwidth. If the data transfer rate is too high, some receivers will lose data, and retransmissions will be required. If the data transfer rate is too slow, an inordinate amount of time will be required to transfer the data. In this paper, we examine an approach toward rate-controlled multicast of bulk data in which the ...

Keywords: bulk data, heterogeneity, multiple multicast groups, rate control

8 A grid service broker for scheduling distributed data-oriented applications on global grids

 Srikumar Venugopal, Rajkumar Buyya, Lyle Winton
October 2004 **Proceedings of the 2nd workshop on Middleware for grid computing MGC '04**
Publisher: ACM Press
Full text available:  pdf(374.36 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Large communities of researchers distributed around the world are engaged in analyzing huge collections of data generated by scientific instruments and replicated on distributed resources. In such an environment, scientists need to have the ability to carry out their studies by transparently accessing distributed data and computational resources. In this paper, we propose and develop a Grid broker that mediates access to distributed resources by (a) discovering suitable data sources for a giv ...

9 Session 9B: Power issues in high level synthesis: An integrated data path optimization for low power based on network flow method

Chun Gi Lyuh, Taewhan Kim, C. L. Liu

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design ICCAD '01**

Publisher: IEEE Press

Full text available:  pdf(305.30 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We propose an effective algorithm for power optimization in behavioral synthesis. In previous work, it has been shown that several hardware allocation/binding problems for power optimization can be formulated as network flow problems and be solved optimally. However, in these formulations, a fixed schedule was assumed. In such context, one key problem is: given an optimal network flow solution to a hardware allocation/binding problem for a schedule, how to generate a new optimal network flow sol ...

10 Session 6D: low power interconnect modeling and optimization: Bus optimization for low-power data path synthesis based on network flow method

Sungpack Hong, Taewhan Kim

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design ICCAD '00**

Publisher: IEEE Press

Full text available:  pdf(142.70 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Sub-micron feature sizes have resulted in a considerable portion of power to be dissipated on the buses, causing an increased attention on savings for power at the behavioral level and RT level of design. This paper addresses the problem of minimizing power dissipated in switching of the buses in data path synthesis. Unlike the previous approaches in which minimization of the power consumed in buses has not been considered until operation scheduling is completed, our approach *integrates the b* ...

11 Parallel processing of near fine grain tasks using static scheduling on OSCAR (Optimally Scheduled Advanced Multiprocessor)

Hironori Kasahara, Hiroki Honda, Seinosuke Narita


November 1990 **Proceedings of the 1990 ACM/IEEE conference on Supercomputing Supercomputing '90**

Publisher: IEEE Computer Society

Full text available:  pdf(1.06 MB) Additional Information: [full citation](#), [abstract](#), [references](#)

This paper proposes a compilation scheme for parallel processing of near fine grain tasks, each of which consists of several instructions or a statement, on a multiprocessor system called OSCAR (Optimally Scheduled Advanced Multiprocessor). The scheme allows us to minimize synchronization and data transfer overheads and to optimally use registers of each processor by using a static scheduling algorithm considering data transfer. This scheme can effectively be combined with macro-dataflow computa ...

12 A taxonomy of Data Grids for distributed data sharing, management, and processing

 Srikumar Venugopal, Rajkumar Buyya, Kotagiri Ramamohanarao

June 2006 **ACM Computing Surveys (CSUR)**, Volume 38 Issue 1

Publisher: ACM Press

Full text available:  pdf(1.70 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Data Grids have been adopted as the next generation platform by many scientific

communities that need to share, access, transport, process, and manage large data collections distributed worldwide. They combine high-end computing technologies with high-performance networking and wide-area storage management techniques. In this article, we discuss the key concepts behind Data Grids and compare them with other data sharing and distribution paradigms such as content delivery networks, peer-to-peer n ...


Keywords: Grid computing, data-intensive applications, replica management, virtual organizations

13 SMASH: a program for scheduling memory-intensive application-specific hardware


Pravil Gupta, Alice C. Parker

May 1994 **Proceedings of the 7th international symposium on High-level synthesis ISSS '94**

Publisher: IEEE Computer Society Press

Full text available:  pdf(610.07 KB) Additional Information: [full citation](#), [references](#), [citations](#)

14 Improved results for data migration and open shop scheduling

 Rajiv Gandhi, Magnús M. Halldórsson, Guy Kortsarz, Hadas Shachnai

January 2006 **ACM Transactions on Algorithms (TALG)**, Volume 2 Issue 1

Publisher: ACM Press

Full text available:  pdf(191.93 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The *data migration* problem is to compute an efficient plan for moving data stored on devices in a network from one configuration to another. We consider this problem with the objective of minimizing the sum of completion times of all storage devices. It is modeled by a transfer graph, where vertices represent the storage devices, and the edges indicate the data transfers required between pairs of devices. Each vertex has a nonnegative weight, and each edge has a release time and a process ...

Keywords: Approximation algorithms, LP rounding, data migration, linear programming, open shop, scheduling

15 Scalable and fault-tolerant support for variable bit-rate data in the exedra streaming server

 Stergios V. Anastasiadis, Kenneth C. Sevcik, Michael Stumm

November 2005 **ACM Transactions on Storage (TOS)**, Volume 1 Issue 4

Publisher: ACM Press

Full text available:  pdf(1.01 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We describe the design and implementation of the Exedra continuous media server, and experimentally evaluate alternative resource management policies using a prototype system that we built. Exedra has been designed to provide scalable and efficient support for variable bit-rate media streams whose compression efficiency leads to reduced storage space and bandwidth requirements in comparison to constant bit-rate streams of equivalent quality. We examine alternative disk striping policies, and qua ...

Keywords: Content distribution, multimedia compression

16 A Framework for Scheduling and Context Allocation in Reconfigurable Computing

R. Maestre, M. Fernandez, R. Hermida, N. Bagherzadeh

November 1999 **Proceedings of the 12th international symposium on System synthesis ISSS '99**

Publisher: IEEE Computer Society

Full text available:  pdf(247.31 KB)

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Reconfigurable computing is emerging as a viable design alternative to implement a wide range of computationally intensive applications. The scheduling problem becomes a really critical issue in achieving the high performance that these kind of applications demands. This paper describes the different aspects regarding the scheduling problem in a reconfigurable architecture. We also propose a general strategy in order to perform at compilation time a scheduling that includes all possible optimiza ...

17 [Simultaneous scheduling and binding for power minimization during](#)



[microarchitecture synthesis](#)

Aurobindo Dasgupta, Ramesh Karri

April 1995 **Proceedings of the 1995 international symposium on Low power design ISLPED '95**

Publisher: ACM Press

Full text available: [pdf\(172.36 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

18 [A Complete Data Scheduler for Multi-Context Reconfigurable Architectures](#)

M. Sánchez-Élez, M. Fernández, R. Maestre, F. Kurdahi, R. Hermida, N. Bagherzadeh

March 2002 **Proceedings of the conference on Design, automation and test in Europe DATE '02**

Publisher: IEEE Computer Society

Full text available: [pdf\(127.63 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#)

A new technique is presented in this paper to improve the efficiency of data scheduling for multi-context reconfigurable architectures targeting multimedia and DSP applications. The main goal is to improve the application execution time minimizing external memory transfers. Some amount of on-chip data storage is assumed to be available in the reconfigurable architecture. Therefore the Complete Data Scheduler tries to optimally exploit this storage, saving data and result transfers between on-chip and ex ...

19 [Scheduling parallel I/O operations](#)



Ravi Jain, Kiran Somalwar, John Werth, J. C. Browne

December 1993 **ACM SIGARCH Computer Architecture News**, Volume 21 Issue 5

Publisher: ACM Press

Full text available: [pdf\(640.28 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

The I/O bottleneck in parallel computer systems has recently begun receiving increasing interest. Most attention has focused on improving the performance of I/O devices using fairly *low-level* parallelism in techniques such as disk striping and interleaving. Widely applicable solutions, however, will require an integrated approach which addresses the problem at multiple system levels, including applications, systems software, and architecture. We propose that within the context of such an ...

20 [Adaptive performance prediction for distributed data-intensive applications](#)



Marcio Faerman, Alan Su, Richard Wolski, Francine Berman

January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '99**

Publisher: ACM Press

Full text available: [pdf\(292.25 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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1 [Media synchronization and QoS packet scheduling algorithms for wireless systems](#)

Azzedine Boukerche, Harold Owens

February 2005 **Mobile Networks and Applications**, Volume 10 Issue 1-2**Publisher:** Kluwer Academic PublishersFull text available: [pdf\(579.10 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Wireless multimedia synchronization is concerned with distributed multimedia packets such as video, audio, text and graphics being played-out onto the mobile clients via a base station (BS) that services the mobile client with the multimedia packets. Our focus is on improving the Quality of Service (QoS) of the mobile client's on-time-arrival of distributed multimedia packets through network multimedia synchronization. We describe a media synchronization scheme for wireless networks, ...

Keywords: distributed algorithms, media synchronization, mobile multimedia, packet scheduling algorithm, quality of service (QoS), wireless communications

2 [Synchronization in multimedia data retrieval](#)

Anna Haj Hać, Cindy X. Xue

January 1997 **International Journal of Network Management**, Volume 7 Issue 1**Publisher:** John Wiley & Sons, Inc.Full text available: [pdf\(487.64 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Synchronization of multiple medium streams in real time has been recognized as one of the most important requirements for multimedia applications based on broadband high-speed networks. This article presents a complete synchronization scheme for distributed multimedia information systems. © 1997 John Wiley & Sons, Ltd.

3 [A taxonomy of Data Grids for distributed data sharing, management, and processing](#)



Srikumar Venugopal, Rajkumar Buyya, Kotagiri Ramamohanarao

June 2006 **ACM Computing Surveys (CSUR)**, Volume 38 Issue 1**Publisher:** ACM PressFull text available: [pdf\(1.70 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Data Grids have been adopted as the next generation platform by many scientific communities that need to share, access, transport, process, and manage large data collections distributed worldwide. They combine high-end computing technologies with high-performance networking and wide-area storage management techniques. In this article, we discuss the key concepts behind Data Grids and compare them with other data sharing and distribution paradigms such as content delivery networks, peer-to-peer n ...

Keywords: Grid computing, data-intensive applications, replica management, virtual organizations

4 Distributed scheduling algorithms to improve the performance of parallel data transfers



Dannie Durand, Ravi Jain, David Tseytlin

September 1994 **ACM SIGARCH Computer Architecture News**, Volume 22 Issue 4

Publisher: ACM Press

Full text available: [pdf\(588.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

The cost of data transfers, and in particular of I/O operations, is a growing problem in parallel computing. A promising approach to alleviating this bottleneck is to schedule parallel I/O operations explicitly. We develop a class of decentralized algorithms for scheduling parallel I/O operations, where the objective is to reduce the time required to complete a given set of transfers. These algorithms, based on edge-coloring and matching of bipartite graphs, rely upon simple heuristics to obtain ...

5 Separated high-bandwidth and low-latency communication in the cluster interconnect Clint



Hans Eberle, Nils Gura

November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing Supercomputing '02**

Publisher: IEEE Computer Society Press

Full text available: [pdf\(235.04 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

An interconnect for a high-performance cluster has to be optimized in respect to both high throughput and low latency. To avoid the tradeoff between throughput and latency, the cluster interconnect Clint has a segregated architecture that provides two physically separate transmission channels: A *bulk channel* optimized for high-bandwidth traffic and a *quick channel* optimized for low-latency traffic. Different scheduling strategies are applied. The bulk channel uses a scheduler that ...

6 A general framework for prefetch scheduling in linked data structures and its application to multi-chain prefetching



Seungryul Choi, Nicholas Kohout, Sumit Pamnani, Dongkeun Kim, Donald Yeung

May 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 2

Publisher: ACM Press

Full text available: [pdf\(2.45 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Pointer-chasing applications tend to traverse composite data structures consisting of multiple independent pointer chains. While the traversal of any single pointer chain leads to the serialization of memory operations, the traversal of independent pointer chains provides a source of memory parallelism. This article investigates exploiting such *interchain memory parallelism* for the purpose of memory latency tolerance, using a technique called *multi--chain prefetching*. Previous work ...

Keywords: Data prefetching, memory parallelism, pointer-chasing code

7 Summary of the Second International Workshop on Network and Operating System Support for Digital Audio and Video



Ralf Guido Herrtwich

April 1992 **ACM SIGOPS Operating Systems Review**, Volume 26 Issue 2

Publisher: ACM Press

Full text available: [pdf\(2.58 MB\)](#) Additional Information: [full citation](#), [index terms](#)

8 Separating data and control transfer in distributed operating systems



Chandramohan A. Thekkath, Henry M. Levy, Edward D. Lazowska

November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the sixth international conference on Architectural support for programming languages and operating systems ASPLOS-VI**, Volume 29 , 28 Issue 11 , 5

Publisher: ACM Press

Full text available: pdf(1.42 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Advances in processor architecture and technology have resulted in workstations in the 100+ MIPS range. As well, newer local-area networks such as ATM promise a ten- to hundred-fold increase in throughput, much reduced latency, greater scalability, and greatly increased reliability, when compared to current LANs such as Ethernet. We believe that these new network and processor technologies will permit tighter coupling of distributed systems at the hardware level, and that distribu ...

9 Summary of the Second International Workshop on Network and Operating System



Support for Digital Audio and Video

Ralf Guido Herrtwich

April 1992 **ACM SIGCOMM Computer Communication Review**, Volume 22 Issue 2

Publisher: ACM Press

Full text available: pdf(2.32 MB)

Additional Information: [full citation](#), [index terms](#)

10 QoS aware multi-channel scheduling for IEEE 802.15.3 networks

Aniruddha Rangnekar, Krishna M. Sivalingam

February 2006 **Mobile Networks and Applications**, Volume 11 Issue 1

Publisher: Kluwer Academic Publishers

Full text available: pdf(612.28 KB)

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From a multimedia applications perspective, there is an ever increasing demand for wireless devices with higher bandwidth to support high data rate flows. One possible solution to support the demand for higher bandwidth is to utilize the full spectrum by simultaneously using multiple channels for transmission. Recent approval by the Federal Communications Commission (FCC) has led to considerable interest in exploiting Ultra Wideband (UWB) access on an unlicensed basis in the 3.1-10.6 GHz band. C ...

11 FM-QoS: real-time communication using self-synchronizing schedules



Kay Connelly, Andrew A. Chien

November 1997 **Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '97**

Publisher: ACM Press

Full text available: pdf(145.06 KB)

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FM-QoS employs a novel communication architecture based on network feedback to provide predictable communication performance (e.g. deterministic latencies and guaranteed bandwidths) for high speed cluster interconnects. Network feedback is combined with self-synchronizing communication schedules to achieve synchrony in the network interfaces (NIs). Based on this synchrony, the network can be scheduled to provide predictable performance without special network QoS hardware. We describe the key el ...


Keywords: communication, network, predictable performance, quality-of-service, real-time, scheduling, synchronization, wormhole

The loosely-synchronous transfer mode

Danilo Florissi

October 1994 **Proceedings of the 1994 conference of the Centre for Advanced Studies on Collaborative research CASCON '94**

Publisher: IBM Press

Full text available:  pdf(74.63 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


This paper overviews the novel Loosely-synchronous Transfer Mode (LTM). In LTM, the network signals sources about its current status, that is, destinations to which frames are being currently routed and quality of service that is being provided. By using the signals, sources schedule frame transmissions to occur when the network is delivering the most adequate service. The Synchronous Protocol Stack (SPS) builds on LTM to deliver synchronization signals from LTM upwards to applications. SPS can ...

13 Memory and network optimization in embedded designs: An efficient scalable and flexible data transfer architecture for multiprocessor SoC with massive distributed memory

Sang-Il Han, Amer Baghdadi, Marius Bonaciu, Soo-Ik Chae, Ahmed A. Jerraya

June 2004 **Proceedings of the 41st annual conference on Design automation DAC '04**

Publisher: ACM Press

Full text available:  pdf(582.06 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Massive data transfer encountered in emerging multimedia embedded applications requires architecture allowing both highly distributed memory structure and multiprocessor computation to be handled. The key issue that needs to be solved is then how to manage data transfers between large numbers of distributed memories. To overcome this issue, our paper proposes a scalable Distributed Memory Server (DMS) for multiprocessor SoC (MPSoC). The proposed DMS is composed of: (1) high-performance and flexi ...


Keywords: data transfer architecture, memory server, message passing, multiprocessor SoC, network interface, network on chip

14 Synchronization and communication in the T3E multiprocessor

Steven L. Scott

September 1996 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 31 , 30 Issue 9 , 5

Publisher: ACM Press

Full text available:  pdf(1.34 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


This paper describes the synchronization and communication primitives of the Cray T3E multiprocessor, a shared memory system scalable to 2048 processors. We discuss what we have learned from the T3D project (the predecessor to the T3E) and the rationale behind changes made for the T3E. We include performance measurements for various aspects of communication and synchronization. The T3E augments the memory interface of the DEC 21164 microprocessor with a large set of explicitly-managed, external r ...

15 Comparing random data allocation and data striping in multimedia servers

Jose Renato Santos, Richard R. Muntz, Berthier Ribeiro-Neto

June 2000 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2000 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '00**, Volume 28 Issue 1

Publisher: ACM Press

Full text available:  pdf(1.18 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We compare performance of a multimedia storage server based on a random data allocation layout and block replication with traditional data striping techniques. Data striping techniques in multimedia servers are often designed for restricted workloads, e.g. sequential access patterns with CBR (constant bit rate) requirements. On the other hand, a system based on random data allocation can support virtually any type of multimedia application, including VBR (variable bit rate) video or audio, ...

16 Supporting sets of arbitrary connections on iWarp through communication context switches



Anja Feldmann, Thomas M. Stricker, Thomas E. Warfel

August 1993 **Proceedings of the fifth annual ACM symposium on Parallel algorithms and architectures SPAA '93**

Publisher: ACM Press

Full text available: pdf(1.27 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



17 Performance study of synchronization schemes on parallel CBR video servers



Chow-Sing Lin, Wei Shu, Min-You Wu

October 1999 **Proceedings of the seventh ACM international conference on Multimedia (Part 2) MULTIMEDIA '99**

Publisher: ACM Press

Full text available: pdf(562.34 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



Keywords: CBR, parallel video server, synchronization

18 A survey of research and practices of Network-on-chip



Tobias Bjerregaard, Shankar Mahadevan

June 2006 **ACM Computing Surveys (CSUR)**, Volume 38 Issue 1

Publisher: ACM Press

Full text available: pdf(1.41 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The scaling of microchip technologies has enabled large scale systems-on-chip (SoC). Network-on-chip (NoC) research addresses global communication in SoC, involving (i) a move from computation-centric to communication-centric design and (ii) the implementation of scalable communication structures. This survey presents a perspective on existing NoC research. We define the following abstractions: system, network adapter, network, and link to explain and structure the fundamental concepts. First, r ...

Keywords: Chip-area networks, GALS, GSI design, NoC, OCP, SoC, ULSI design, communication abstractions, communication-centric design, interconnects, network-on-chip, on-chip communication, sockets, system-on-chip



19 Performance study of a clustered shared-memory multiprocessor



K. B. Irani, A. R. Naji

June 1988 **Proceedings of the 2nd international conference on Supercomputing ICS '88**

Publisher: ACM Press

Full text available: pdf(1.32 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A shared-memory multiprocessor having clusters of processing elements and memory modules is considered. Each cluster has two others as its neighbors. The clusters are interconnected in such a way that the memory modules of a cluster can also be accessed by the processors of the neighboring clusters besides its own processors through its cluster interconnection network. The processors and memories of all clusters are also connected to a shared interconnection network. This permits pr ...



20 Optimistic replication

Yasushi Saito, Marc Shapiro

March 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 1**Publisher:** ACM Press

Full text available: pdf(656.72 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Data replication is a key technology in distributed systems that enables higher availability and performance. This article surveys optimistic replication algorithms. They allow replica contents to diverge in the short term to support concurrent work practices and tolerate failures in low-quality communication links. The importance of such techniques is increasing as collaboration through wide-area and mobile networks becomes popular. Optimistic replication deploys algorithms not seen in tradition ...

Keywords: Replication, disconnected operation, distributed systems, large scale systems, optimistic techniques

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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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